

Notice of References Cited	Application/Control No. 09/865,847		Applicant(s)/Patent Under Reexamination KAXIRAS ET AL.	
	Examiner Chun Cao		Art Unit 2115	Page 1 of 1

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	B	US-6,473,814	10-2002	Lyons et al.	710/35
	C	US-6,385,697	05-2002	Miyazaki, Mitsuhiro	711/128
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NON-PATENT DOCUMENTS

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	U	"Automatic Cache Line Access Monitoring" IBM TDB, Vol. 37, No. 6A, June 1994, page 299.
	V	K. Stein, et al., "Storage Array and Sense/Refresh Circuit for Single Transistor Memory Cells", IEEE Journal of Solid State Circuits, Vol. SC-7, No. 5, 336-340 (October 1972).
	W	K. Stein, et al., Session V: Memory II, "Storage Array and Sense/Refresh Circuit for Single Transistor Memory Cells", IEEE International of Solid State Circuits conference, 1972, pages 56-57.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.